PO-CHUN CHIEN

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RESEARCH INTERESTS

Formal Verification: Soft/Hard-ware Model Checking, QBF/SAT Solving, Automata Theory
Electronic Design Automation (EDA): Logic Synthesis & Optimization, Computation Models

SKILLS

Programming: proficient in **C/C++, Python, VerilogHDL**, Cadence Skill, MATLAB
Language: Mandarin Chinese, English (IELTS 7.5, TOEFL 103, GRE 155/170/4.0)

EDUCATION

Ph.D. in Informatics (Computer Science), LMU Munich *from July 2021*

· A member of SoSy-Lab led by Prof. Dr. Dirk Beyer.

M.S. in Electronics Engineering, National Taiwan University (NTU) *Sep. 2018–June 2020*

· Overall GPA: 4.22/4.30. A member of ALCom Lab led by Prof. Jie-Hong Roland Jiang.

B.S. in Electrical Engineering, NTU *Sep. 2015–June 2018*

· Overall GPA: 4.16/4.30 (top 5%).

ACADEMIC/CONTEST AWARDS

2nd place in the IWLS 2021 Programming Contest *July 2021*
2020 Institute of Information & Computing Machinery Master's Thesis Excellence Award *Mar. 2021*
2020 Lam Research Master's Thesis Excellence Award at NTU *Nov. 2020*
1st place in the 2020 Chinese Institute of Electrical Engineering Thesis Award *Oct. 2020*
1st place in the 2019 ICCAD CADathlon *Nov. 2019*
1st place in the Formosa Grand Challenge "Taking with AI" *Mar. 2019*
NTU Presidential Award * 2 semesters *Sep. 2016–June 2017*

WORK EXPERIENCES

Research Assistant in SoSy-Lab at LMU Munich *from July 2021*
Research Assistant in ALCom Lab at NTU *July–Nov. 2020, April–June 2021*
Teaching Assistant of "Introduction to EDA" at NTU *Spring 2019, Spring 2020*
Teaching Assistant of "DL for Human Language Processing" at NTU *Fall 2018*
Teaching Assistant of "Advanced Deep Learning" at NTU *Spring 2018*
Summer Intern at MediaTek ADCT/PDK Dept. *Hsinchu, July–Aug. 2018*

PUBLICATIONS

[1] Y.-N. Wang, Y.-R. Luo, **P.-C. Chien**, P.-L. Wang, H.-R. Wang, W.-H. Lin, J.-H. R. Jiang, and C.-Y. R. Huang, "Compatible Equivalence Checking of X-Valued Circuits," in *Proc. ICCAD*, 2021. To appear.
[2] S. Rai, W. L. Neto, ..., **P.-C. Chien**, and ..., "Logic Synthesis Meets Machine Learning: Trading Exactness for Generalization," in *Proc. DATE*, 2021.
[3] **P.-C. Chien** and J.-H. R. Jiang, "Time Multiplexing via Circuit Folding," in *Proc. DAC*, 2020.
[4] **P.-C. Chien**, "Circuit Folding: From Combinational to Sequential Circuits," Master's thesis, National Taiwan University, 2020.

[5] **P.-C. Chien** and J.-H. R. Jiang, "Time-Frame Folding: Back to the Sequentiality," in *Proc. ICCAD*, 2019.

RESEARCH PROJECTS

Machine Learning + Logic Synthesis (II) *April–July 2021*

- Learn multi-output Boolean circuits for CIFAR-10 image classification under different size constraints.
- For smaller circuits: ensemble of binary decision trees via one-against-one approach.
- For larger circuits: quantized CNN with grouped convolutions synthesized with sub-adder sharing.
- We won the **2nd place** in the IWLS 2021 Programming Contest.

Compatible Equivalence Checking of X-valued Circuits *July 2020–July 2021*

- Verify the equivalence of 2 X-valued (ternary logic) netlists, with the X-values serving as don't cares.
- Construct the miter circuit with dual-rail encoding, and adopt various optimization techniques.
- Identify and utilize the compatible equivalence relations of internal signals to guide the SAT solver.

Machine Learning + Logic Synthesis *May–Dec. 2020*

- Learn an unknown Boolean function from a training set consisting of input-output pairs.
- The learned function is in the form of And-Inverter Graph with strict hardware cost (≤ 5000 gates).
- Methods: decision tree with fringe-feature detection, and neural network with pruning and quantization.
- We achieved the highest testing accuracy for the most number of benchmarks in the IWLS 2020 Contest.

Time Multiplexing (TM) via Circuit Folding *Nov. 2019–July 2020*

- The research manuscript was accepted and published by **DAC 2020**.
- TM is an important technique to overcome the I/O bandwidth bottleneck of FPGAs.
- Our new formulation achieves TM through structural and functional circuit folding at the logic level.
- Experiments show the effectiveness of the structural method and improved optimality of the functional method on look-up-table and flip-flop usage.

Time-Frame Folding (TFF): Back to the Sequentiality *Sep. 2018–Nov. 2019*

- The research manuscript was accepted and published by **ICCAD 2019**.
- TFF is the reverse operation of time-frame expansion. It constructs a sequential circuit from an k-iterative combinational circuit.
- The constructed circuit is equivalent to the original circuit within the bounded k time-frames.
- Empirical evaluation demonstrates its ability in circuit size compaction and suggests potential use in testbench generation and bounded strategy generalization.

Formosa Grand Challenge "Taking with AI" *June 2018–Mar. 2019*

- A nationwide ML competition hosted by Taiwan Ministry of Science and Technology.
- The goal is to build a conversational AI agent that understands Mandarin Chinese.
- Our team **ranked 1st** in the competition and won the final prize.

RELATED COURSES

Verif.	SoC Verification, Logic Synthesis & Verification, Algorithms
EDA	VLSI Testing, Physical Design, Data Structure & Programming
ML	ML & have it deep and structured, Advanced DL, DL for Human Language Processing
Others	Advanced Computer Architecture, Digital Signal Processing, Introduction to Cryptography